The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-29. (Canceled)

30. (Previously Presented) A semiconductor device comprising:

a substrate having at least one driving circuit comprising a plurality of thin film transistors, clock lines for supplying clock signals to the driving circuit, at least one wiring line crossing the clock lines, a first insulating film and a second insulating film,

wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors, and an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors,

wherein said wiring line is formed over the first and second insulating films,

wherein said upper layer is formed between the first and second insulating films, and

wherein said lower layer extends in a same direction as said upper layer.

31. (Previously Presented) A device according to claim 30, wherein an interval between adjacent ones of the clock lines is wider than a width of each of the clock lines.

32. (Previously Presented) A device according to claim 30, wherein said clock lines are connected to a shift register circuit in the driving circuit.

33. (Previously Presented) A device according to claim 30, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

34. (Previously Presented) A device according to claim 30, wherein said wiring line formed over the upper layer is connected to the upper layer.

35. (Previously Presented) A device according to claim 30, further comprising black matrices over the thin film transistors, wherein said wiring line is made of the same layer as the black matrices.

36. (Previously Presented) A semiconductor device comprising:

a substrate having at least one driving circuit comprising a plurality of thin film transistors, clock lines for supplying clock signals to the driving circuit, at least one wiring line crossing the clock lines, a first insulating film and a second insulating film,

wherein each of the clock lines or each of base portions of the clock lines is made of a two-layer structure, a lower layer of said two-layer structure comprising the same wiring material as gate electrodes of the thin film transistors, and an upper layer of said two-layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors,

wherein said wiring line is formed over the first and second insulating films,

wherein said upper layer is formed between the first and second insulating films, and

wherein the second insulating film is thicker than the first insulating film.

37. (Previously Presented) A device according to claim 36, wherein an interval between adjacent ones of the clock lines is wider than a width of each of the clock lines.

38. (Previously Presented) A device according to claim 36, wherein said clock lines are connected to a shift register circuit in the driving circuit.

39. (Previously Presented) A device according to claim 36, further comprising a pixel portion comprising a plurality of thin film transistors on said substrate.

40. (Previously Presented) A device according to claim 36, wherein said wiring line formed over the upper layer is connected to the upper layer.

41. (Previously Presented) A device according to claim 36, wherein said lower layer extends in a same direction as said upper layer.

42. (Previously Presented) A device according to claim 36, further comprising black matrices over the thin film transistors, wherein said wiring line is made of the same layer as the black matrices.